

1 **IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

2 Serial No.
3 Filing Date
4 Inventorship Andrews
5 Applicant Microsoft Corporation
6 Attorney's Docket No. MS1-1378US
7 Title: Methods and Systems for Transparent Depth Sorting

8 **INFORMATION DISCLOSURE STATEMENT**

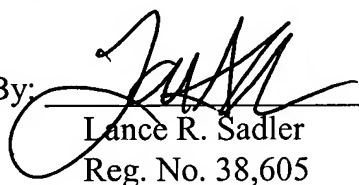
9 *References -- See Attached Form PTO-1449*

10 **REMARKS**

11 The citations listed, copies attached, are submitted in compliance with the
12 duty of disclosure defined in 37 CFR §1.56. The Examiner is requested to make
13 these citations of official record in this application.

14 Respectfully Submitted,

15 Date: 9/12/03

16 By: 
17 Lance R. Sadler
18 Reg. No. 38,605

Please type a plus sign (+) inside this box → +



Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
		Application Number			
		Filing Date			
		First Named Inventor		Andrews	
		Group Art Unit			
		Examiner Name			
		Attorney Docket Number		MS1-1378US	
Sheet	2	of	2		

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		YAMACHI, et al.; "The Technique for Object and Collision Detection by Z-buffer"; Department of Computer and Information Engineering; Nippon Institute of Technology; Vol. 43; No. 6; June 2002; pp. 1899-1911.	
		WHITE, et al; "The Tayra 3-D Graphics Raster Processor; Comput. & Graphics, Vol. 21; No. 2; pp. 129-142; 1997	
		BRESENHAM; "Teaching the graphics processing pipeline: cosmetic and geometric attribute implications"; Computers & Graphics 25 (2001) 343-349; 7pages.	
		DOCTOR, et al; "Using raster scan in color graphics"; Mini-Micro Systems; December 1981; pp. 101-108	
		WHITTED; "Hardware Enhanced 3-D Raster Display System"; CMCCS '81/ACCHO '81; pp. 349-356	
		FUCHS et al; "Pixel-Planes: A VLSI-Oriented Design For 3-D Raster Graphics"; CMCCS '81/ACCHO'81; pp. 343-347	
		PARKE; "Simulation and Expected Performance Analysis of Multiple Processor Z-Buffer Systems"; 1980 ACM 0-89791-021-4/80/0700-0048; pp. 48-56	
		CHEN et al.; "Reduce the Memory Bandwidth of 3D Graphics Hardware With a Novel Rasterizer"; Journal of Circuits, Systems, and Computers, Vol. 11; No. 4; (2002) pp. 377-391	

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ² Applicant is to place a check mark here if English language Translation is attached.

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